

AN10044

Handling Reset in the ISP116x

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Application note

Document information

Info	Content
Keywords	ISP1160, ISP1160/01, ISP1161, ISP1161A, ISP1161A1, host controller, peripheral controller, USB, universal serial bus
Abstract	This document explains the reset pulse condition in the ISP116x. Remark: ISP116x denotes any Philips USB single-chip host and peripheral controller whose name starts with 'ISP116'; this includes ISP1160, ISP1160/01, ISP1161, ISP1161A, ISP1161A1 and any future derivative.

Revision history

Rev	Date	Description
01	20040920	First release.

Contact information

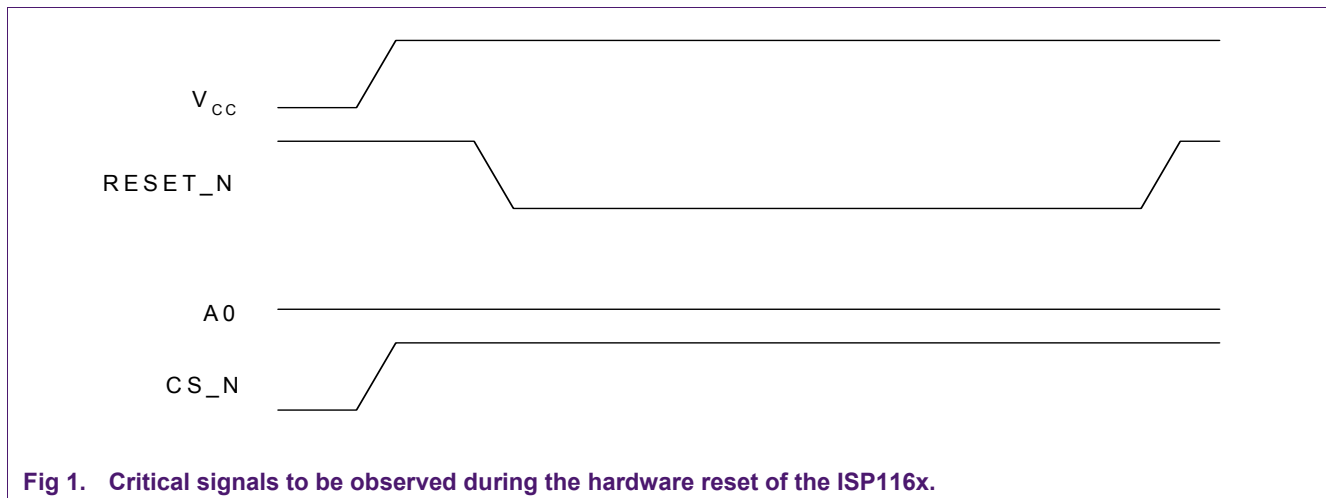
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1. Introduction

It is important to provide a correct reset pulse condition to the ISP116x. [Fig 1](#) shows the critical signals that must be observed during the hardware reset of the ISP116x.



The sequence in [Fig 1](#) can be explained as:

1. V_{CC} is provided to the ISP116x.
2. Shortly after, the reset signal is provided to the ISP116x.
3. A0 maintains a LOW level.
4. CS_N maintains a deasserted state.

Remark: During the reset assertion, do not have any pulse on the CS_N and A0 pins.

2. Power-on reset configuration

The ISP116x has an internal power-on reset (POR) circuitry, enabling the RESET_N pin to be connected as shown in [Fig 2](#). This configuration will perform a power-on reset for the ISP116x in applications in which the CPU does not need to control the ISP116x reset.

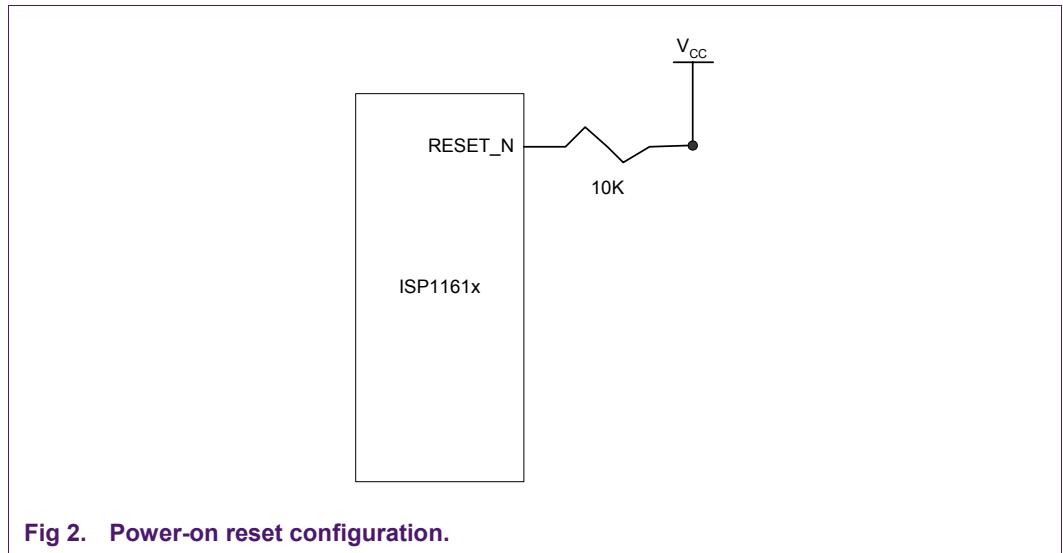


Fig 2. Power-on reset configuration.

Remark: If the RESET_N pin is not handled appropriately, the ISP116x may enter into an unknown condition.

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